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Found adding within 1 word of legs (+ transistor).

First 6 results of about 8 from 2 queries.

ABSTRACT Merritt, Carey Reid. A Pneumatically Actuated Brace ... [distance: 1]

A single NPN **transistor** switches the solenoid valve on/off by using a digital

... **Adding the Legs:** 4. Connect the four 18" pieces of wood to the body so ...

<http://crim.ece.ncsu.edu/assets/publications/thesis/merritt2003-thesis/merritt2003-thesis.pdf> -- [Cached](#) - [Similar pages](#)

Boing Boing: May 2005 [distance: 0]

A Carnegie Mellon engineer is in the early stages of **adding legs** to a ... a guide to producing podcasts, and rebuilding an old **transistor** guitar amp. ...

http://boingboing.net/2005_05_01_archive.html - 513k - [Cached](#) - [Similar pages](#)

Information Technology News for week 22 / 2005 [distance: 0]

Single Molecule **Transistor** A Reality. Source: Slashdot Org latest news headlines

... A Carnegie Mellon engineer is in the early stages of **adding legs** to a ...

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Robotic Nation Evidence [distance: 0]

... announced the fabrication of a **transistor** from a single organic molecule. ...

But Sitti is hoping that **adding legs** to the capsule will give physicians a ...

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Robotic Nation Evidence: 06/01/2005 - 06/30/2005 [distance: 0]

... announced the fabrication of a **transistor** from a single organic molecule. ...

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THE AIR FORCE INSTITUTE OF TECHNOLOGY (AFIT) MEMS INTERFEROMETRIC ... [distance: 1]

Page 1. ...

<http://research.airuniv.edu/papers/ay2000/afit/afit-ge-eng-00m-18.pdf> -- [Cached](#) - [Similar pages](#)

Triode Systems - wfsection-A Simple Multi Filter Block Idea [distance: 1]

... especially **transistor** types and even more so if they are mono-block, ...

You could expand this idea by **adding extra legs** in the circuit for other ...

<http://www.triode-systems.com/modules/wfsection/article.php?articleid=10> - 16k - [Cached](#) - [Similar pages](#)

Z-Walker mk III [distance: 0]

Adding legs to the walker is maybe the most crucial part of the whole design.

... A PNP has a symbol with the arrow pointing inwards and a NPN **transistor** ...

<http://vsim.freesevers.com/walk-kit.html> - 43k - [Cached](#) - [Similar pages](#)

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IEEE JNL IEEE Journal or Magazine


IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

 
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Zhiyong Liang; Jianping Wu; Ke Xu;
Computer Networks and Mobile Computing, 2003. ICCNMC 2003. 2003 International Conference on
20-23 Oct. 2003 Page(s):128 - 135
[AbstractPlus](#) | Full Text: [PDF](#)(4257 KB) IEEE CNF
- ☐ **2. How to obtain more compactable channel routing solutions**
Cong, J.; Wong, D.F.;
Design Automation Conference, 1988. Proceedings., 25th ACM/IEEE
12-15 June 1988 Page(s):663 - 666
[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) IEEE CNF
- ☐ **3. Reducing cache miss ratio for routing prefix cache**
Huan Liu;
Global Telecommunications Conference, 2002. GLOBECOM '02. IEEE
Volume 3, 17-21 Nov. 2002 Page(s):2323 - 2327 vol.3
[AbstractPlus](#) | Full Text: [PDF](#)(403 KB) IEEE CNF
- ☐ **4. Building block routing-a symbolic approach**
Chen, N.-P.;
Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988
16-19 May 1988 Page(s):11.2/1 - 11.2/4
[AbstractPlus](#) | Full Text: [PDF](#)(388 KB) IEEE CNF
- ☐ **5. High performance CMOS macromodule layout synthesis**
Jaewon Kim; Kang, S.M.; Sapatnekar, S.S.;
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on
Volume 4, 30 May-2 June 1994 Page(s):179 - 182 vol.4
[AbstractPlus](#) | Full Text: [PDF](#)(464 KB) IEEE CNF
- ☐ **6. An efficient building block layout methodology for compact placement**
Bourbakis, N.G.; Mortazavi, M.;
VLSI, 1995. Proceedings., Fifth Great Lakes Symposium on
16-18 March 1995 Page(s):118 - 123
[AbstractPlus](#) | Full Text: [PDF](#)(428 KB) IEEE CNF
- ☐ **7. Geometric compaction on channel routing**
Cheng, C.-K.; Deutsch, D.N.; Shohara, C.; Taparuskas, M.; Bubien, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 11, Issue 1, Jan 1992 Page(s):115 - 127
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(((legs <near/2> transistor) <and> compaction)<in>metadata)

IEEE JNL IEEE Journal or Magazine

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IEEE JNL IEEE Journal or Magazine

Display Format: ☒ Citation ☐ Citation & Abstract

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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((compaction)<in>metadata)

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- ☐ 1. **Optimal zero-aliasing space compaction of test responses**
 Chakrabarty, K.; Murray, B.T.; Hayes, J.P.;
 Computers, IEEE Transactions on
 Volume 47, Issue 11, Nov. 1998 Page(s):1171 - 1187
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(972 KB\)](#) IEEE JNL
- ☐ 2. **Dynamic test compaction for synchronous sequential circuits using static compaction techniques**
 Pomeranz, I.; Reddy, S.M.;
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 25-27 June 1996 Page(s):53 - 61
[AbstractPlus](#) | Full Text: [PDF\(740 KB\)](#) IEEE CNF
- ☐ 3. **Bottleneck removal algorithm for dynamic compaction and test cycles reduction**
 Chakradhar, S.T.; Raghunathan, A.;
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 18-22 Sept. 1995 Page(s):98 - 104
[AbstractPlus](#) | Full Text: [PDF\(812 KB\)](#) IEEE CNF
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 18-23 Oct. 1998 Page(s):954 - 961
[AbstractPlus](#) | Full Text: [PDF\(772 KB\)](#) IEEE CNF
- ☐ 5. **Design of optimum multi-dimensional energy compaction filters**
 Damara-Venkata, N.; Tuqan, J.; Evans, B.L.;
 Signals, Systems and Computers, 2002. Conference Record of the Thirty-Sixth Asilomar Conference on
 Volume 1, 3-6 Nov. 2002 Page(s):350 - 354 vol.1
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 Chakrabarty, K.;
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 Volume 17, Issue 5, May 1998 Page(s):452 - 457
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- ☐ 7. **Improving the efficiency of static compaction based on chronological order enumeration of test sequences [logic testing]**
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